WHAT IS CLAIMED IS:

1. An upconverting circuit comprising:

a clock for defining a sequence of input polyphase cycles;

a polyphase component generator that provides N_p polyphase components at each input polyphase cycle, wherein $N_p>2$;

a memory that stores said polyphase components from at least one polyphase cycle prior to the current polyphase cycle;

a plurality of filters, each filter processing a plurality of said polyphase components stored in said memory to generate a filtered polyphase component corresponding to that filter; and

a multiplexer that outputs said filtered polyphase components in a predetermined order to generate a filtered output signal.

2. The upconverting circuit of Claim 1 wherein each filter utilizes the same functional relationship to generate said filtered polyphase components.

3. The upconverting circuit of Claim 1 wherein said memory comprises a shift register.

4. The upconverting circuit of Claim 1 wherein said filters are finite impulse response filters.

5. The upconverting circuit of Claim 1 wherein said filters generate a filtered polyphase component that depends on a non-linear combination of said polyphase components.

6. The upconverting circuit of Claim 1 wherein said polyphase component generator receives one pair of digital signals in each polyphase cycle.